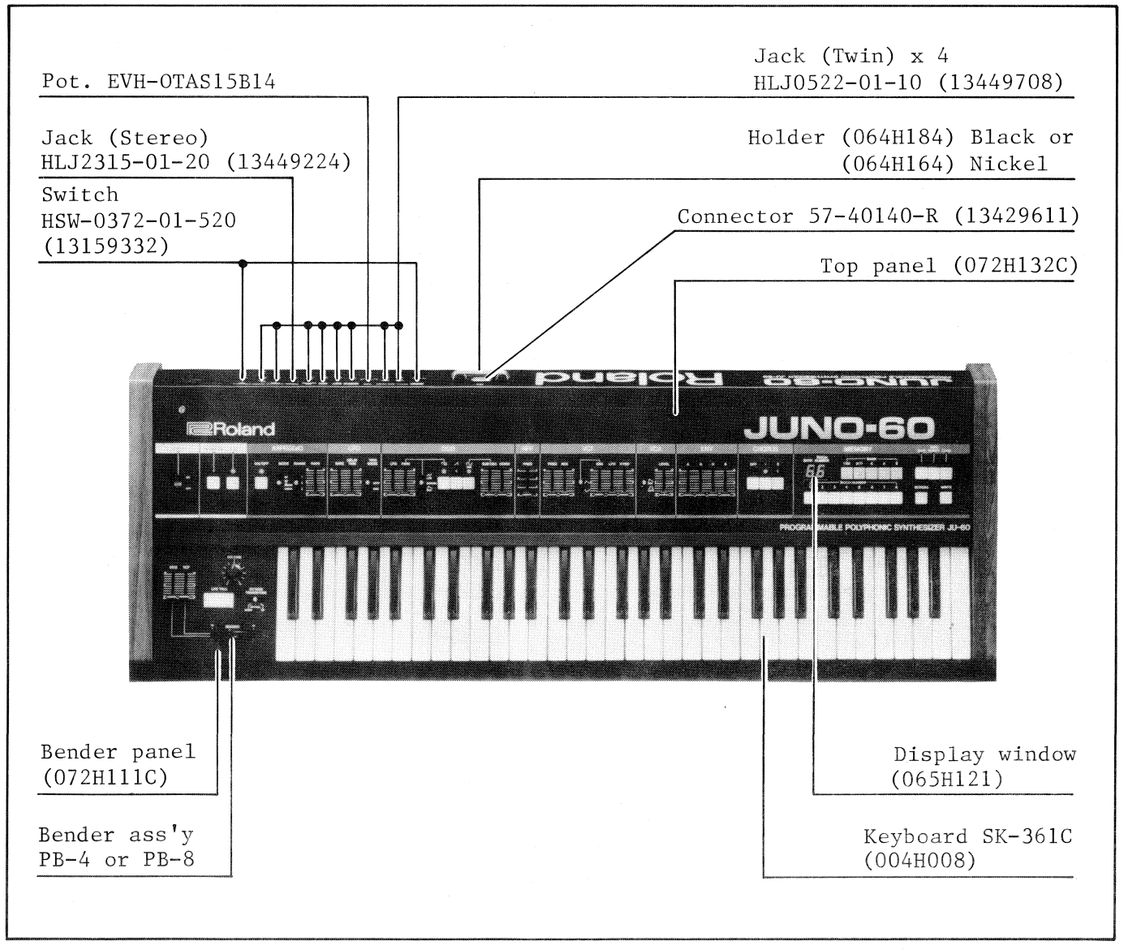
JUNO-60 SERVICE NOTES *First Edition*

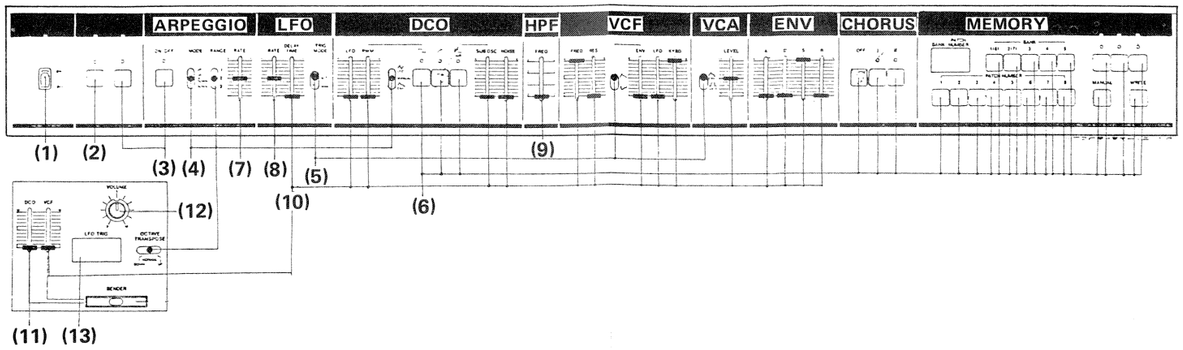
SPECIFICATIONS

Keyboard	61 keys, 5 octaves	
VCF	RESONANCE	(0 – Self Oscillation)
	KEY Follow	(0 – 100%)
ENV	ATTACK Time	(1ms – 3s)
	DECAY Time	(2ms – 12s)
	SUSTAIN Level	(0 – 100%)
	RELEASE Time	(2ms – 12s)
LFO	RATE	(0.3– 20Hz)
	DELAY TIME	(0 – 1.5s)
ARPEGGIO	RATE	(1.5– 50Hz)
MEMORY	PATCH NUMBER	(1 – 8)
	BANK	(1 – 7)

Rear Panel	Output Level (L: –30dBm/M: –15dBm/H: 0dBm)
	ARPEGGIO CLOCK Input (1 step/ pulse= +2.5V or more)
	TUNE (±50 Cents)
Dimensions	1060 x 378 x 113mm
(W x D x H)	41–3/4 x 14–7/8 x 4–7/16in.
Weight	12kg/26lbs. 7oz.
Power Consumption	30W

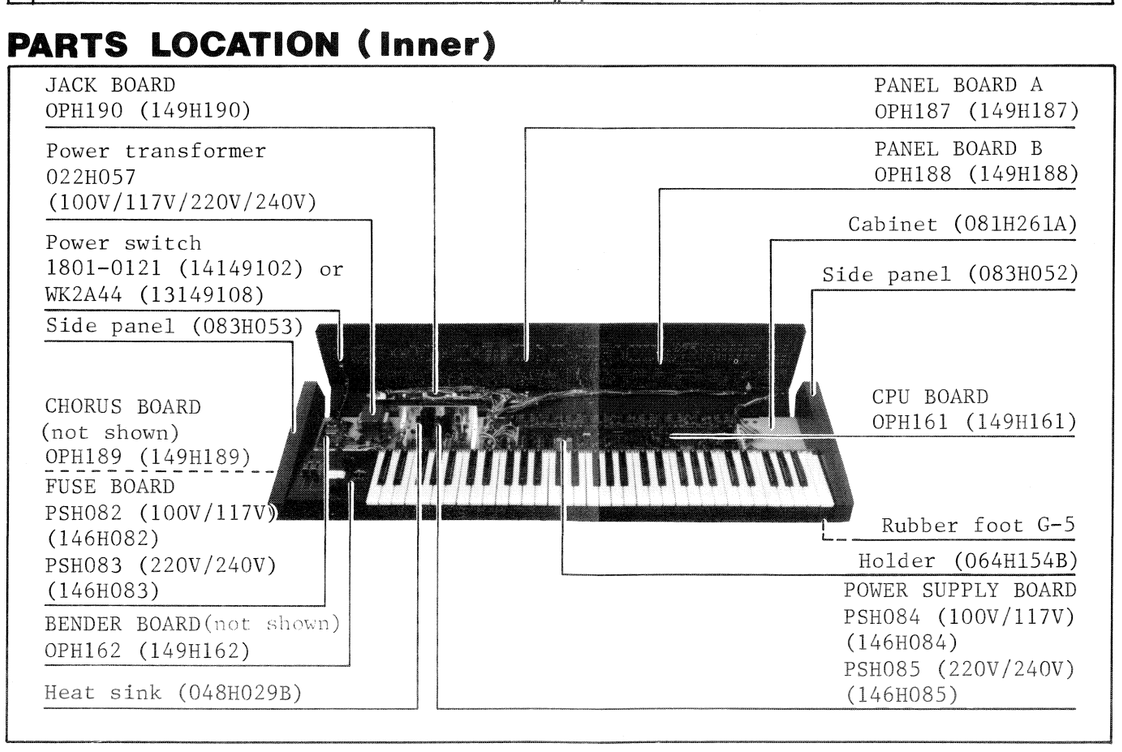
PARTS LOCATION (Top)



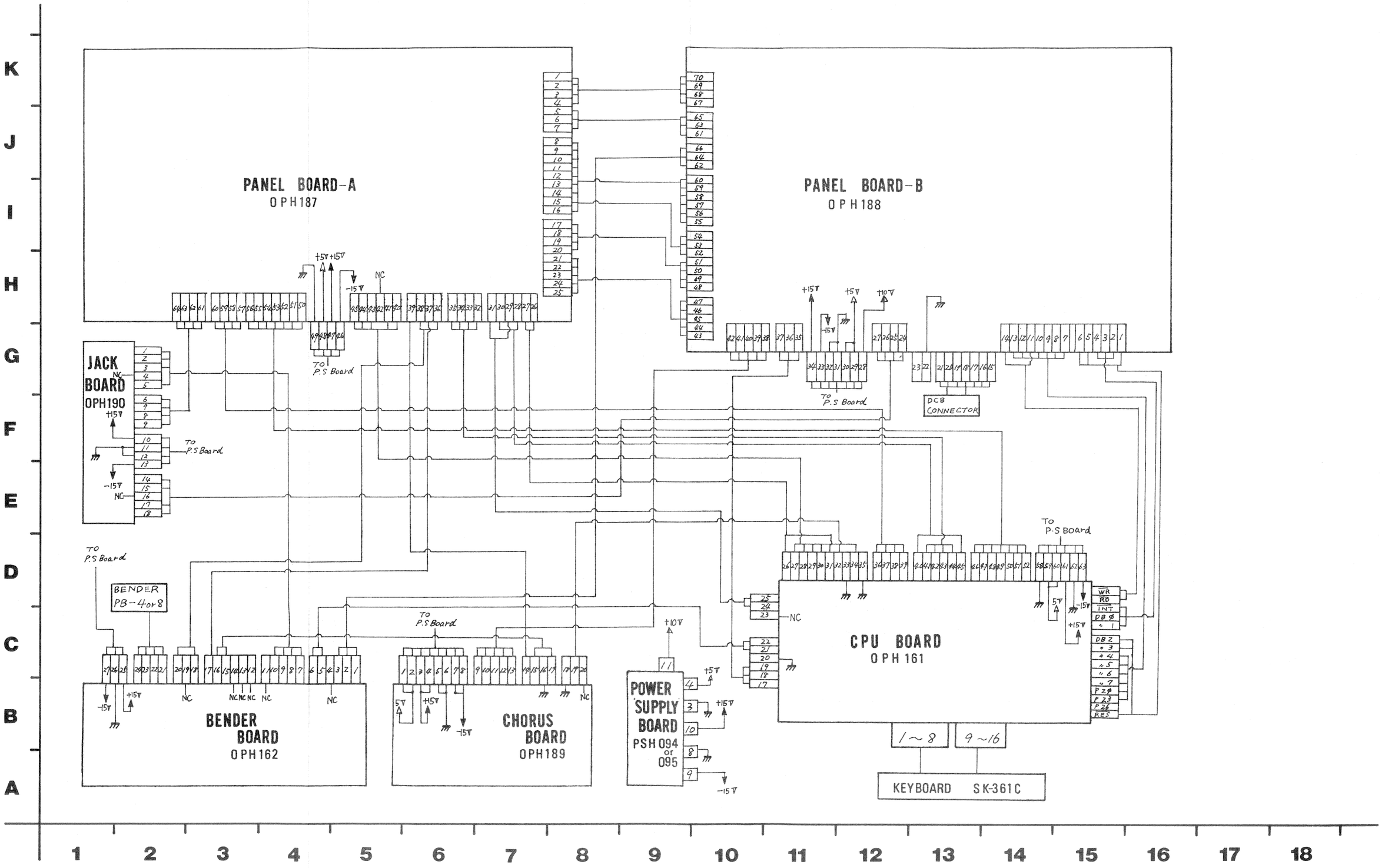


1	Switch 1801-0121 (13149102)		7	Pot. EVA-TOHC14A161MA (13339418)	Knob (016H004)
2	Switch SUT11A-1 (13129321)	Button	8	Pot. EVA-TOHC14A5450KA (13339410)	
3	Switch SUT11A-2 (13129322)	Orange (016H029)	9	Switch EVA-A03C14AGA (13159505)	
		Yellow (016H030)	10	Pot. EVA-TOHC14B5450KB (13339419)	
		White (016H036)	11	Pot. EVA-TOHC14A1410KA (13339416)	
4	Switch SLE-623-18P (13139135)		12	Pot. EWJ-EJAP20B1410KBX2 (13219759)	Knob (22470128)
5	Switch SLE-622-18P (13139136)		13	Switch ass'y KEH10003 (13129717) Switch (KEH10903) (See p. 13.)	
6	Switch KEJ10901 (13169605)	Button			
		Orange (016H037)		ALL LEDs TLR124 (15029103)	
		Yellow (016H038)			
		Grey (016H043)			
		White (016H044)			

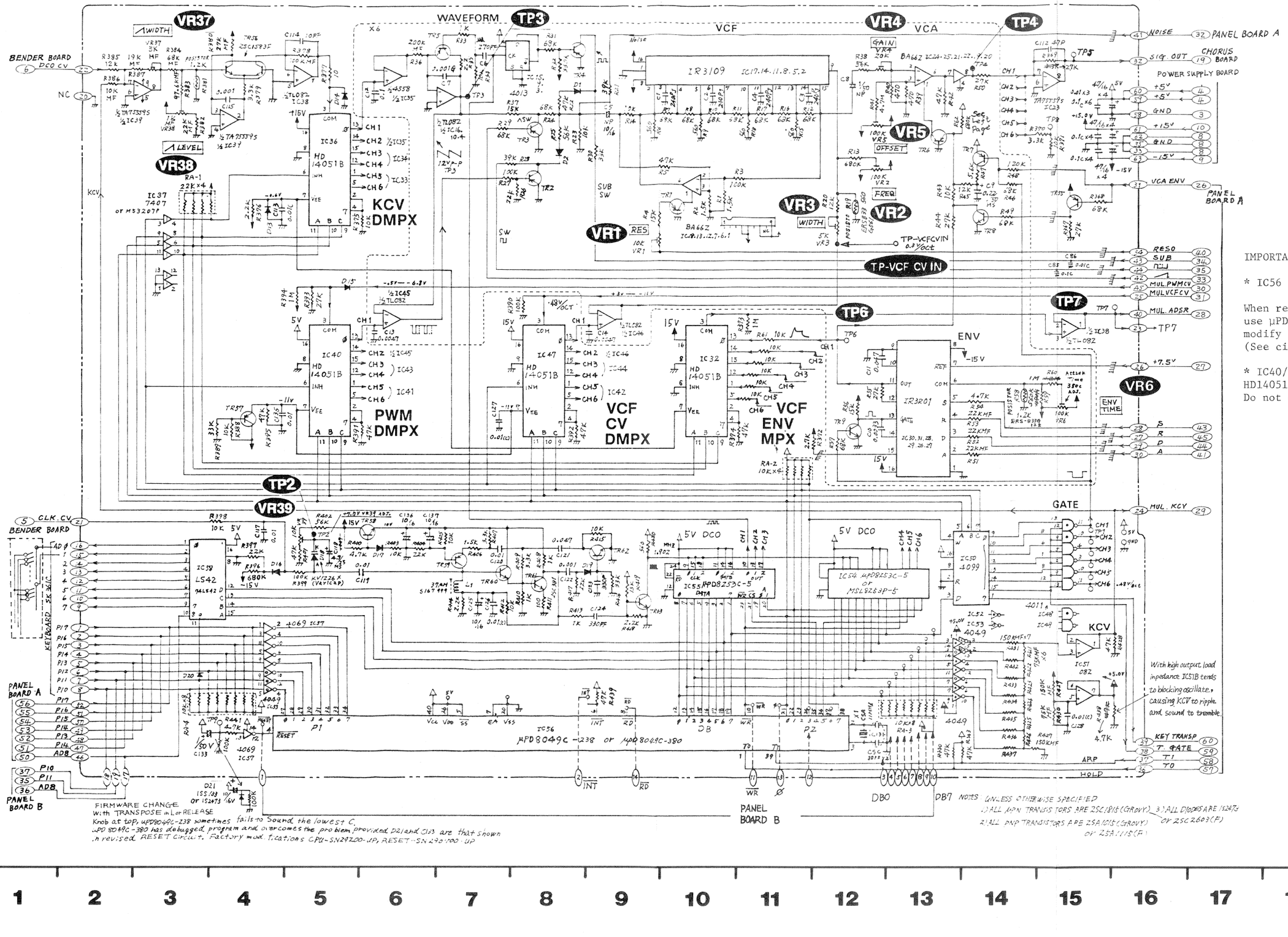
PARTS LOCATION (Inner)



INTERCONNECTION DIAGRAM



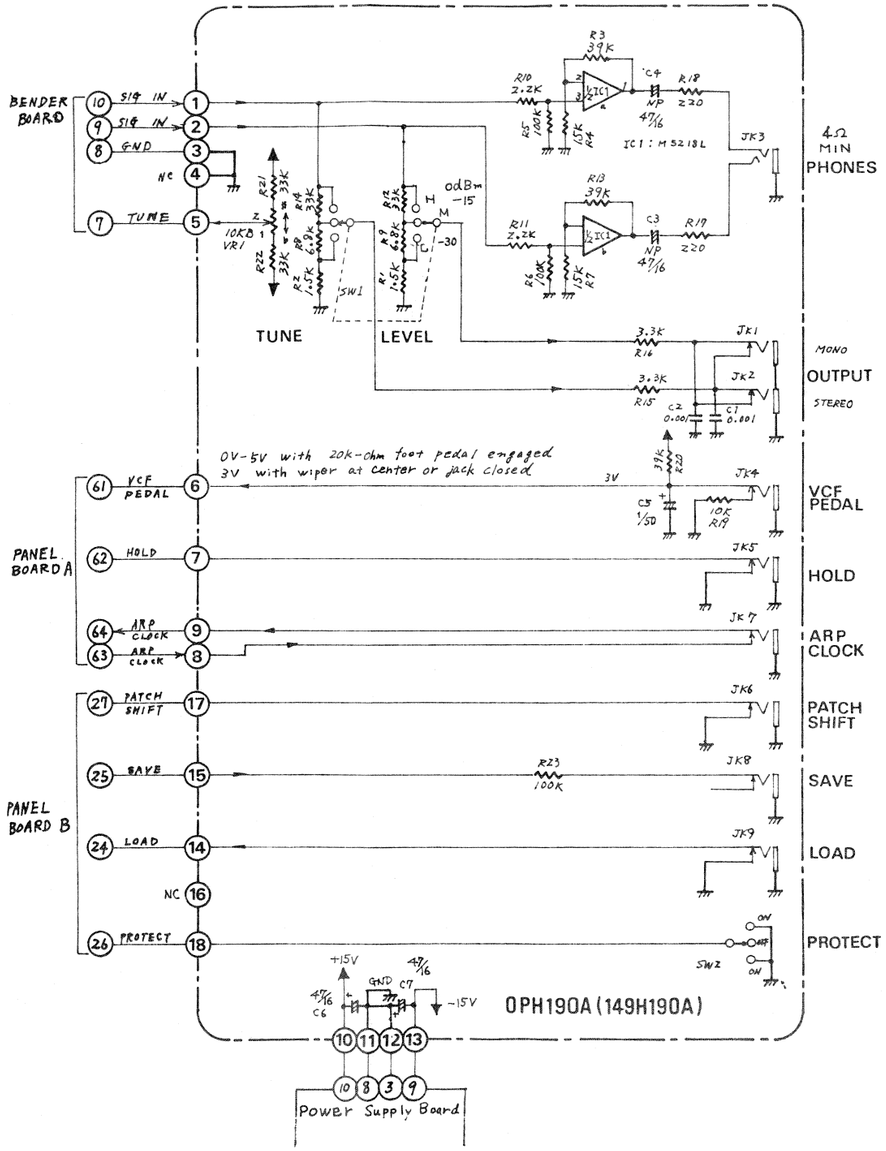
CPU BOARD



IMPORTANT (IC changes)

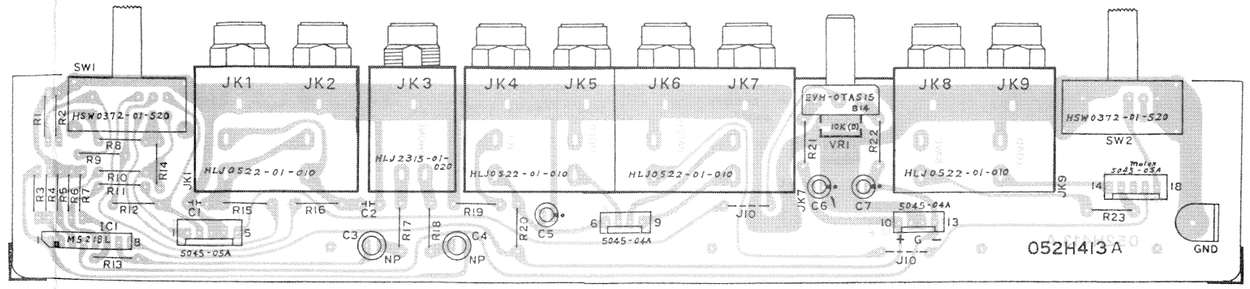
* IC56 (μPD8049C-238 to μPD8049C-380)
When replacing μPD8049C-238, use μPD8049C-380 version and modify RESET circuit. (See circuit diagram.)

* IC40/IC47
HD14051B only.
Do not use equivalents.



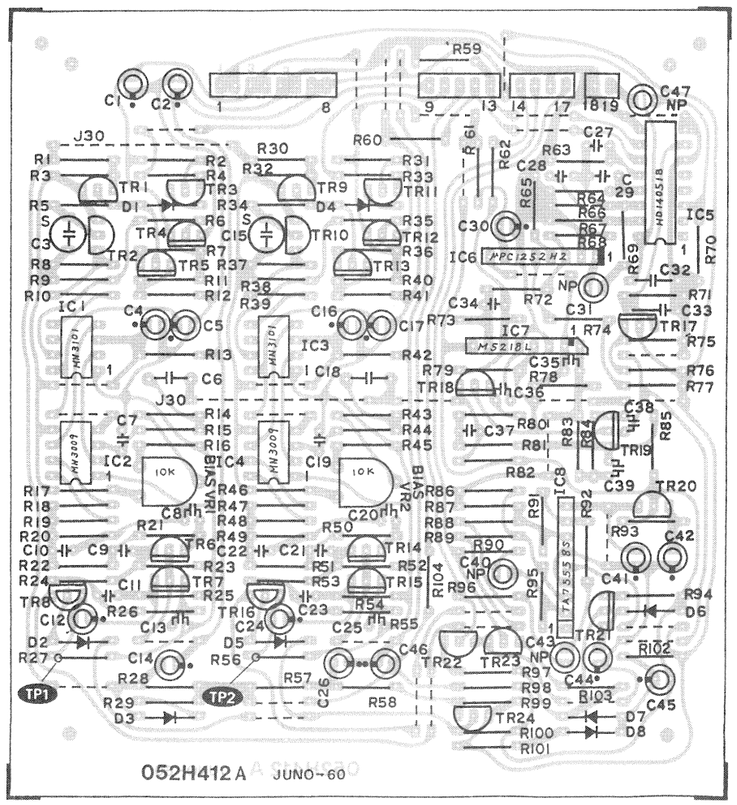
JACK BOARD

OPH190A (149H190A) (pcb 052H413A)

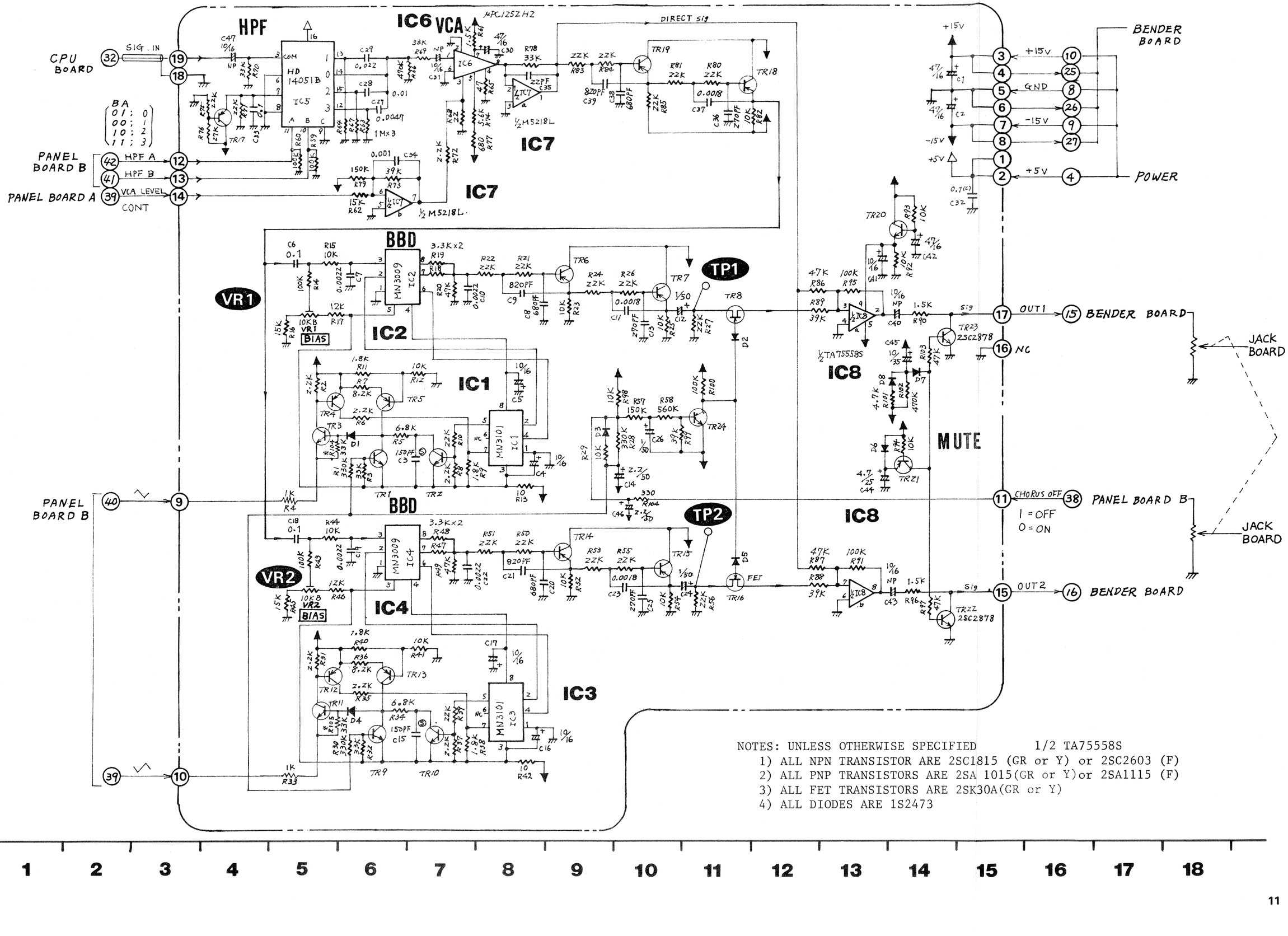


CHORUS BOARD

OPH189A (149H189A) (pcb 052H412A)

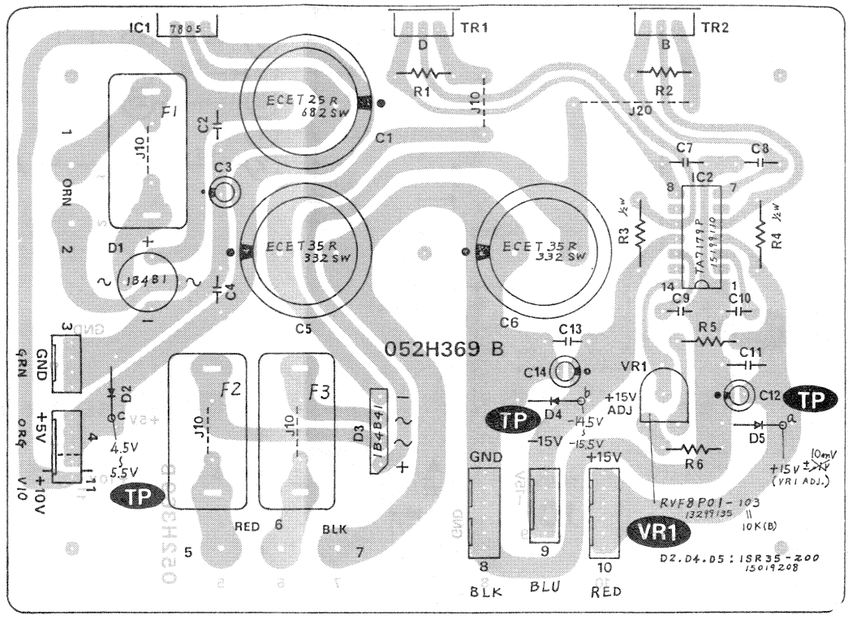


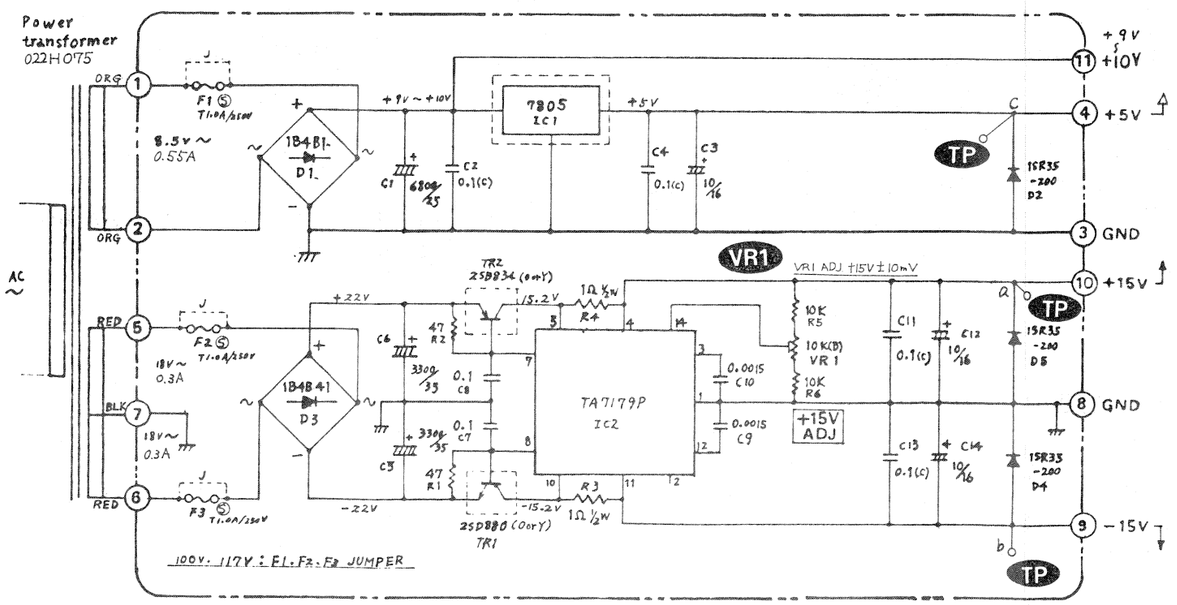
CHORUS BOARD



POWER SUPPLY BOARD

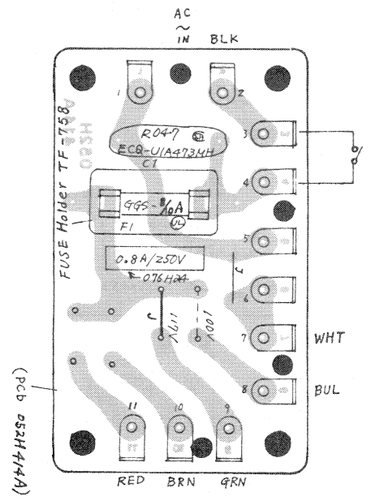
PSH094B (146H094B) 100/117V
PSH095B (146H095B) 220/240V
(pcb 052H369B)

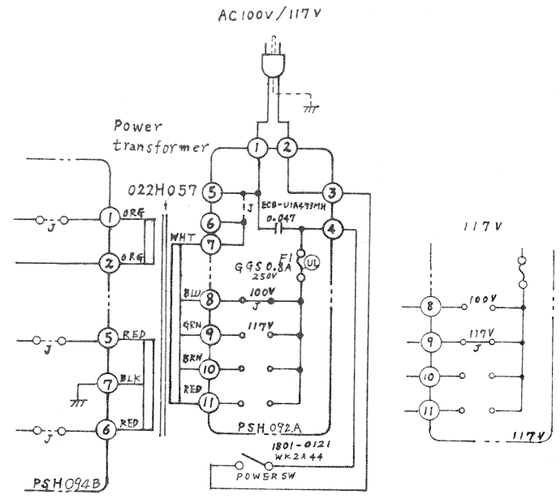




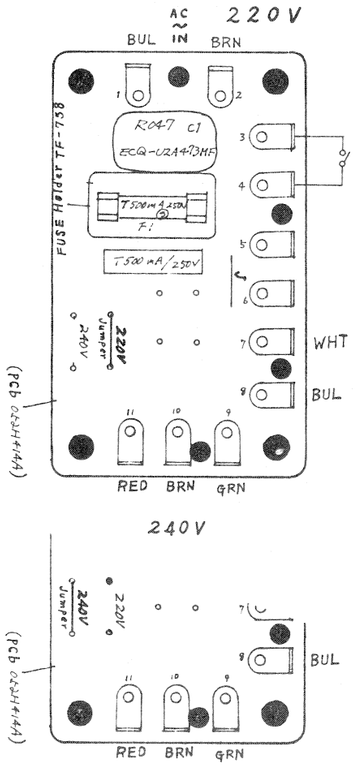
FUSE BOARD

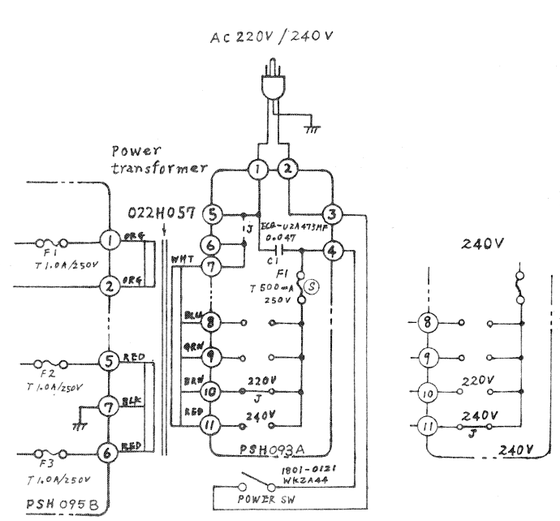
PSH092A (146H092A) 100/117V





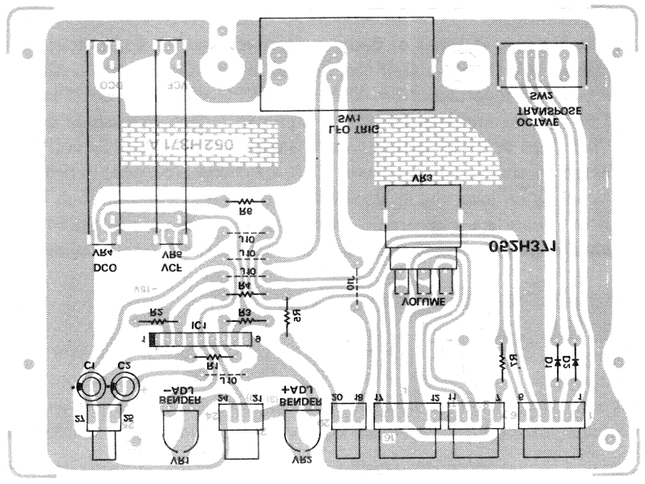
PSH093A (146H093A) 220/240V
(pcb 052H414A)



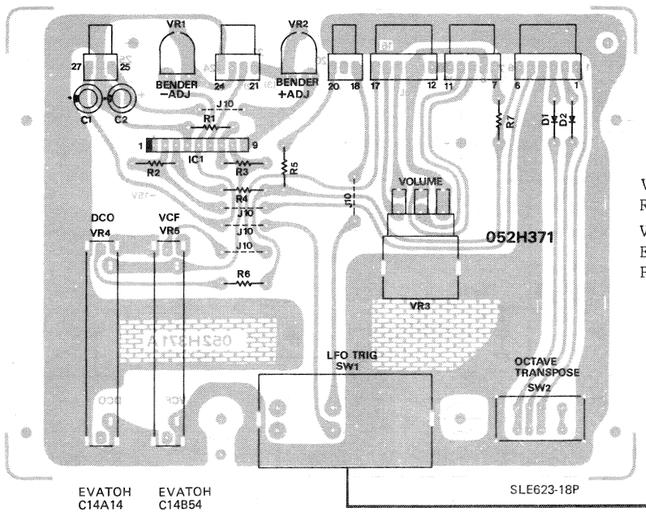


BENDER BOARD

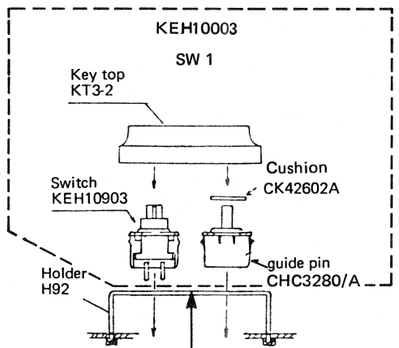
OPH162A (149H162A) (pcb 052H371A)



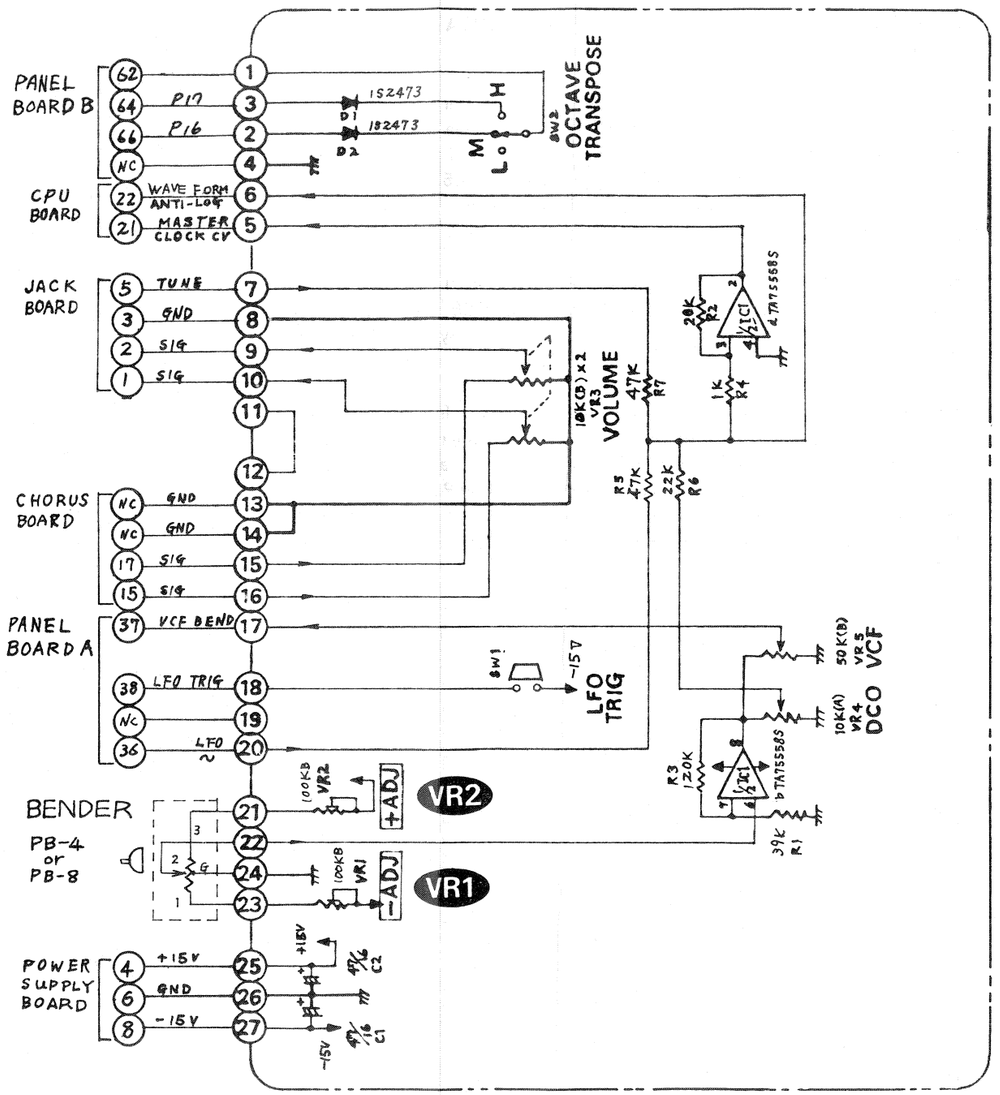
View from foil side



VR1, VR2
RVF8P01-104
VR3
EWJEJA
P20B14



View from component side



CPU BOARD

KEYBOARD AND SWITCH (NON PROGRAMMABLE) SCANNING

The CPU IC58 on the CPU Board applies sequential scanning data (in the leftmost column in Table 1 below) to Address Decoder IC58, setting its appropriate output pin low. Each pin will be connected to port 1 through switch contacts being closed and through inverters IC53 and IC57. The combination of highs and lows at port 1 (pins) tells the CPU which key is pressed, not pressed, or which position the switches are set.

Note: TRANSPOSE switch on Bender Board is not read directly but through SW LATCH IC9 on Panel Board B. TRANSPOSE is scanned beforehand together with the programmable switches by another CPU on Panel Board B.

The CPU IC56 stores two kinds of program for use in different applications, and knows its application at the very first of the scanning cycle. After power on reset, the CPU first issues bits 1001 (see bottom of Table 1) and knows that voices to be assigned to keys played are 6 (L, H, L at Port P10–P12) and that the model it is now installed is the JUNO-60 (L at P17). If the CPU malfunctions, voltages on these port pins and associated circuits (including D20) should be checked.

BUS 6543	PORT-1 0	1	2	3	4	5	6	7
0000	C	C#	D	D#	E	F	F#	G
0001	G#	A	A#	B	C	C#	D	D#
0010	E	F	F#	G	G#	A	A#	B
0011	C*	C#	D	D#	E	F	F#	G
0100	G#	A(442)	A#	B	C	C#	D	D#
0101	E	F	F#	G	G#	A	A#	B
0110	C	C#	D	D#	E	F	F#	G
0111	G#	A	A#	B	C	(C#)	(D)	(D#)
1000	TRANSPOSE		ARP & KEY ASSIGN		ARP RANGE		ARP ON	KEYTRANS
1001	L	H	L	not in use				L

Table 1

KEY ASSIGNMENT

Six channels are assigned to the keys played in the order CH1–CH6, in the cyclic manner, that is, when the 7th key is played while previously played 6 keys are still held, the 7th key steals the first voice.

Three more assignment modes are provided for test purpose. See Adjustment section of this manual.

DIGITAL COMMUNICATION

The JUNO-60 is furnished with a DCB interface for linking with external digital instruments. When the DCB interface circuit on Panel Board B is engaged in communication, it coordinates the transfer of data between two instruments by applying Low to INT of the CPU on the CPU Board (will be detailed under DCB Interface section).

SOUND SOURCE

When a key is played on the keyboard, the CPU (CPU BOARD) provides a set of independent data – Divisor for the programmable counters (IC54, IC55) and CV for WAVEFORM and VCF, to keep the voices sound alike with pitch differences corresponding to a key held.
Fig. 1 shows a simplified block diagram of sound source system, for clarity.

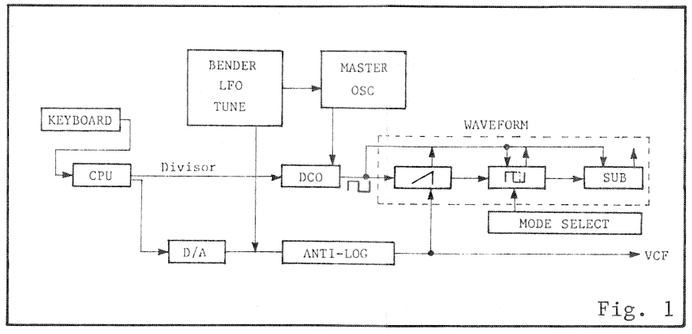


Fig. 1

Master Oscillators TR58-TR62

An LC oscillator having a variable capacitance diode (D18) to which control voltages from BENDER, LFO and TUNE, – common to all the VCOs, are supplied.

Variable range:
BENDER . . . . . ±700 cents
LFO . . . . . ±300 cents
TUNE . . . . . ±50 cents
When these voltages are summed together, the maximum shiftable range of the master oscillator is ±1050 cents or from 1MHz to 3.5MHz with the center frequency at approximately 1.9MHz. The output signal is routed to programmable counters IC54 and IC55 through TR63.

Programmable Counters IC54 and IC55

Programmable counter 8253 containing three 16-bit counters is capable of dividing high frequency signals, generated at the Master oscillator, by up to 65535. Assume that the master oscillator runs at 1902810Hz and a divisor is 4305, the counter develops 442Hz rectangular signals.
Each time key(s) is played, the CPU extracts division data for that key from the internal PROM and delivers it to DATA IN of the counters in 8 bit x 2 format.

Waveform Conversion

SAWTOOTH GENERATOR

Analog voltages (a series of 6 key control voltages for 6 channels) from D/A converter will change in 0.48/oct steps as different keys are played. KCVs are combined with voltages from TUNE, and LFO and BENDER if any, and are fed to anti-log amplifier TR56. The summed voltage increases or decreases in 1V/oct steps at TR56 output, which is passed on to one of S/Hs (IC33-IC35) selected by analog Demultiplexer IC36. C7 charges (current) in proportion to CV coming on inverting input pin of IC16 and discharges through TR5 at the rate of square wave generated from programmable counter (IC54 or IC55), maintaining the sawtooth amplitude constant over the frequency range.

VARIABLE PULSE WIDTH

Besides its direct application as sound source, sawtooth generator also serves as a source for asymmetrical square wave. Sawtooth wave is routed to (–) pin of comparator/S&H circuit where the voltage on (+) pin determines the sampling period of the sawtooth wave thus duty cycle of the square wave.

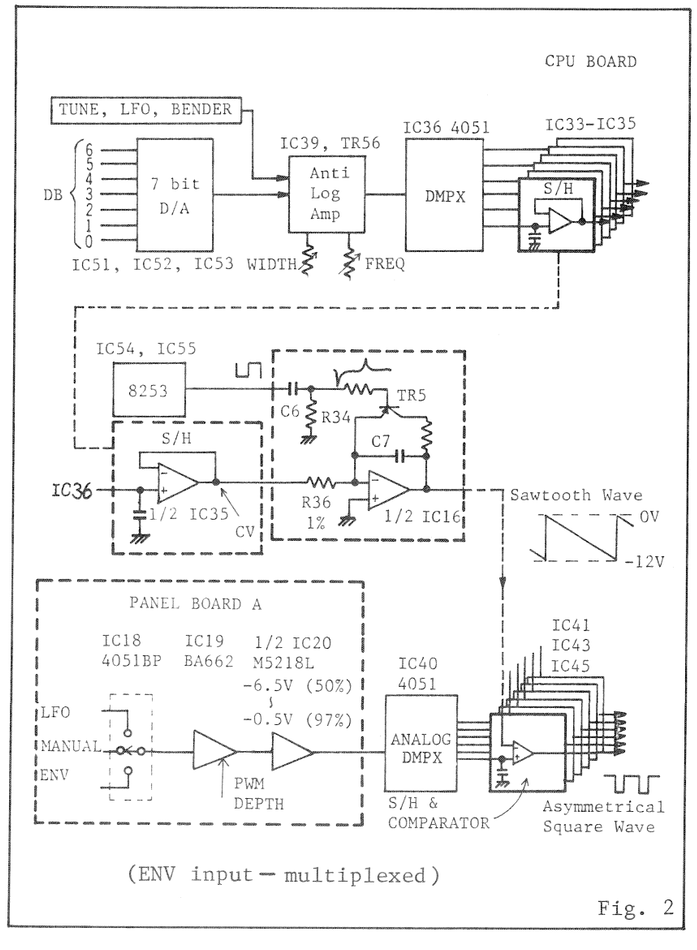


Fig. 2

SUB OSCILLATOR

Square wave from programmable counter is also delivered to flip-flop where it is divided in half, and applied to TR4 base. The amplitude of TR4 output can continuously be varied by setting of SUB VR20 on Panel Board A.

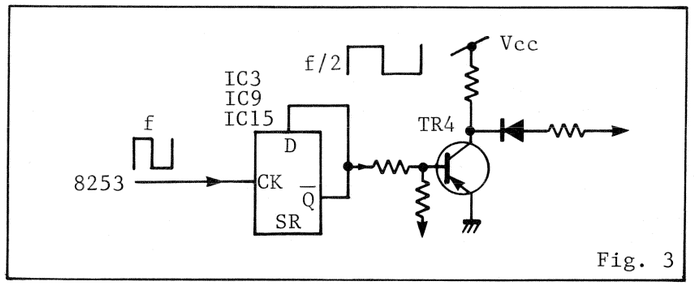


Fig. 3

VCF Control Voltages

While 6 contour voltages developed at ENV generator are running directly to mated VCAs on the exclusive line, they are multiplexed and carried through a common bus together with other control signals for VCF application. On the input pin of summing amp there is another multiplexed voltage (KCV) from D/A converters IC51-IC53 on CPU Board. These multiplexings are synchronized for stable data travel.

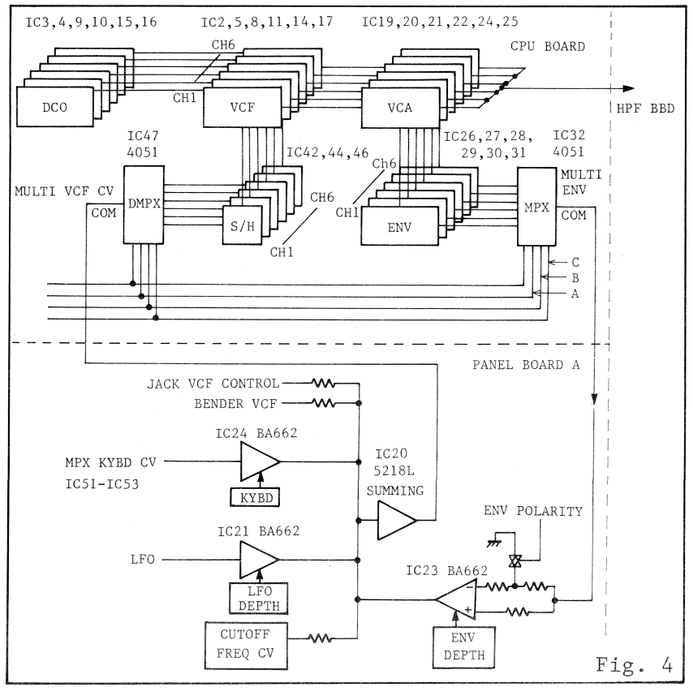


Fig. 4

PANEL BOARD B

CPU μPD80C49C–028

DESIGNATION	PIN NO.	FUNCTION
DB (Data Bus) DBφ	12	Prog SW Scan Display Drive / RAM Address / RAM Data / Slider and Switch Data / A/D Data
1	13	
2	14	
3	15	
4	16	
5	17	
6	18	
7	19	
PORT 1 P1φ	27	Prog SW Read / Display LED Drive
11	28	
12	29	
13	30	
14	31	
15	32	
16	33	
17	34	
PORT 2 P2φ	21	4051 x 4 Address (MPX, DMPX)] RAM x 2 Address
1	22	
2	23	
3	24	Chip Select 4051 CS x 4 40174B, TC40H273P WR Enable
4	35	
5	36	
6	37	
7	38	Tape Interface Output
XTAL-1	2	Inputs for Internal Clock Oscillator
XTAL-2	3	
$\overline{RESET}$	4	Reset Pulse Input
Tφ	1	Tape Interface Input
T1	39	A/D Comparator Input
INT	6	Protect SW Input (Low = Protect ON, High = Protect OFF)
$\overline{RD}$	8	RAM Read Pulse
$\overline{WR}$	10	RAM Write Pulse, 40174, 40H273 Latch Pulse
ALE	11	Address Latch Pulse

Table 2

The flowchart (Fig. 5) will be an aid in reading the description in this section.

① When a new BANK/PATCH button is pressed, the CPU calls "Read RAM" subroutine.
When BANK, PATCH and WRITE buttons are pressed, the CPU calls "Write RAM" routine.

② When the CPU finds a certain amount of descrepancy between the preceding reading and the new reading, it sets Edit Flag and updates the data being delivered.

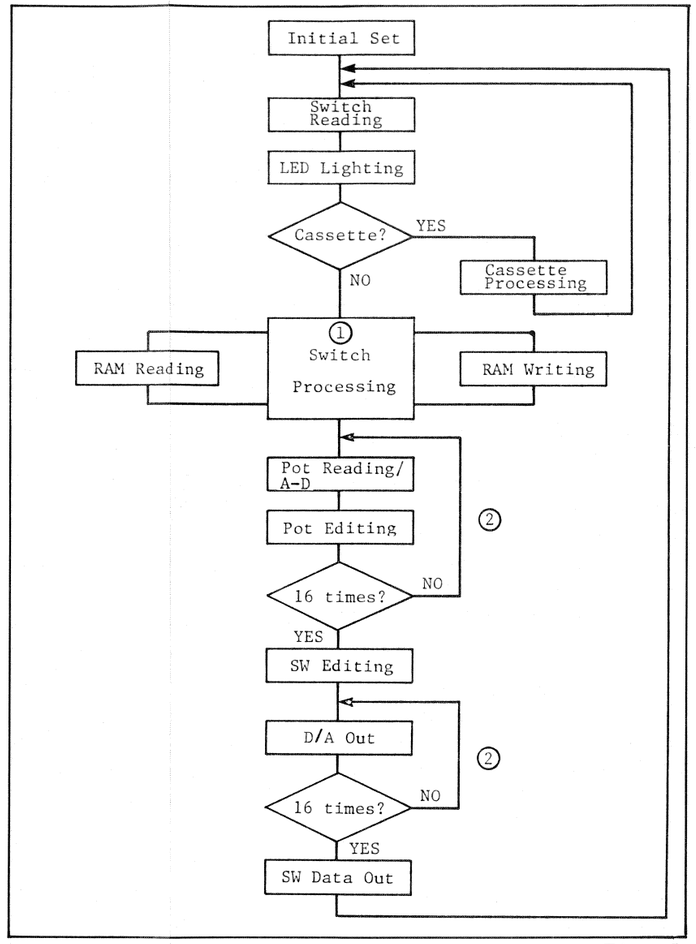


Fig. 5

SWITCH READING

The matrices for the programmable switches and memory switches are located on Panel Boards A, B and Bender Board. They are bussed together on Panel Board B. The bus is divided into five sections with maximum eight switches per section. Each bus section and switch contact are connected to the CPU on Panel Board B: bus section through Latch IC15 (latched on PROG) and through Decoder IC16; contact through Port 1.
The CPU maintains a serial data output (from DB) and reads the resultants from Port 1, in the same manner as described previously under KEY SCANNING.

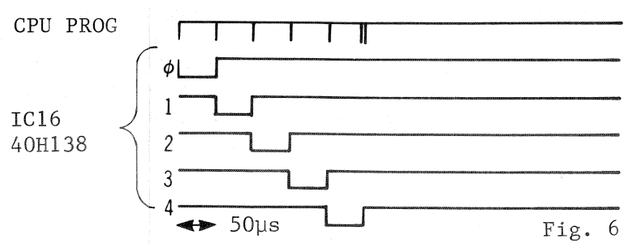


Fig. 6

40H -138	PORT-1 0	1	2	3	4	5	6	7
0	Manual	Write	Save	Verify	Load	not used	not used	not used
1	1	2	Bank Number 3	4	5	not used	not used	not used
2	1	2	Patch Number 3	4	5	6	7	8
3	Chorus 1	WAVEFORM Pulse/Sawtooth/SUB			Chorus 2	Chorus OFF	Transpose L/M/H/HH	
4	ENV Polarity	PWM MODE ENV/MAN/LFO		HPF Cutoff Freq		VCA ENV	Patch Shift	TRIG MODE

Table 3

SWITCH DATA OUTPUT

Of the switches read during the above switch scanning, 11 programmable switches are organized in 14 bit group in the CPU and are divided into two fields when being sent out from the CPU. At the very end portion of the program loop, the CPU first issues 6-bit data on the data bus and IC13 latches it into IC8 with ALE. Then the next 8-bit is directly fed to IC9. IC8 and IC9 latch out 14 bit data at the same time when the Port 2 presents bits X1110XXX.

It should be noted that TRANSPOSE information only is routed to and involved in the CPU Board switch matrix for further processing, while the remaining switch data are delivered directly to respective destinations.

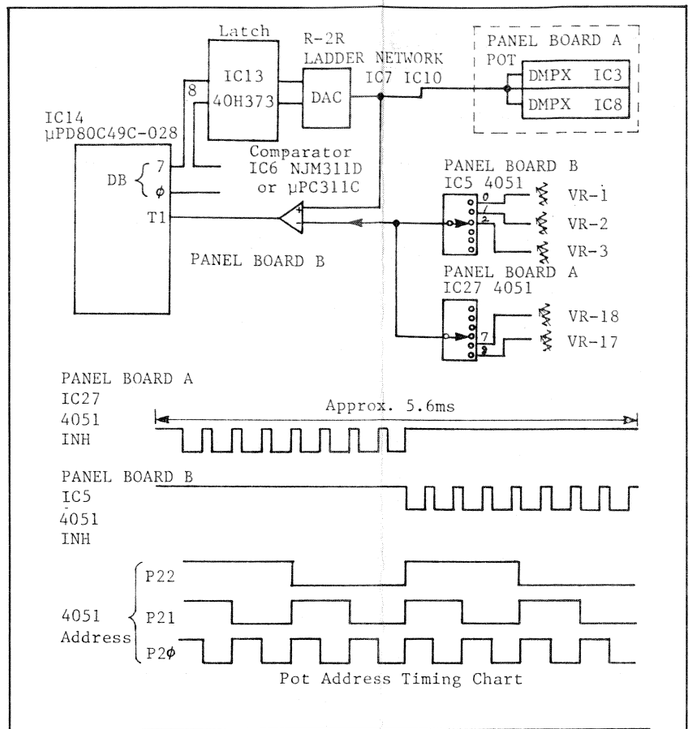
	IC PIN NUMMBER	SW FUNCTION	IC8,IC9 OUTPUT			
IC8 40174B	10	VCA ENV SEL	0=⎍, 1=⎍			
	12	HPF CUTOFF FREQ.	0	0	1	1
	15		0	1	2	3
			1	0	0	1
	9	PWM MODE	0	0	1	1
			LFO	MAN	ENV	X
	5		0	1	0	1
	2	ENV POLARITY	0=∩, 1=∪			
IC9 40H273	5	TRANS-POSE	0	0	1	1
			L	M	H	X
	2		0	I	0	1
	12	LFO TRIGGER	0=AUTO, 1=MAN			
	19	CHORUS 2	0=ON, 1=OFF			
	15	SUB OSC ON/OFF	0=ON, 1=OFF			
	16	⎍ ON/OFF	0=ON, 1=OFF			
	9	⎍ ON/OFF	0=ON, 1=OFF			
	6	CHORUS 1	0=ON, 1=OFF			

Table 4

POTENTIOMETER MULTIPLEXERS AND ADC (PANEL BOARDS A, B)

MULTIPLEXER

All 16 programmable pots are divided between Panel Boards A and B, with each 8 pot group connected to an associated Pot Multiplexer. Pot MPX and ADC (Analog to Digital Converter) allow the computer on the Panel Board B to read and therefore to store the knob settings into RAM for a patch. Addresses specifying the pots to be sampled are fed from Port 2 as shown in Fig. 7. Pot MPX program starts with VR17 DELAY TIME when INH is applied from Latch IC19 on Panel Board B. The MPXer IC27 (Board A) sequentially connects each pot wiper (on Board A) to the ADC which represents analog equivalent of Pot Value in 8 bit format.



	VR	PARAMETER	PORT 2 6 5 4 3	2	1	φ
PANEL BOARD B	1	VCF Env Depth	1 0 0 0	0	0	0
	2	VCF LFO Depth		0	0	1
	3	VCF KYBD Follow		0	1	0
	4	VCA Level		0	1	1
	5	Env Attack		1	0	0
	8	Env Release		1	0	1
	6	Env Decay		1	1	0
	7	Env Sustain		1	1	1
PANEL BOARD A	22	Cutoff Freq	1 0 0 1	0	0	0
	21	Noise Level		0	0	1
	20	Sub OSC Level		0	1	0
	23	Resonance		0	1	1
	19	Pulse Width		1	0	0
	16	LFO Rate		1	0	1
	18	DCO LFO Depth		1	1	0
	17	Delay Time		1	1	1

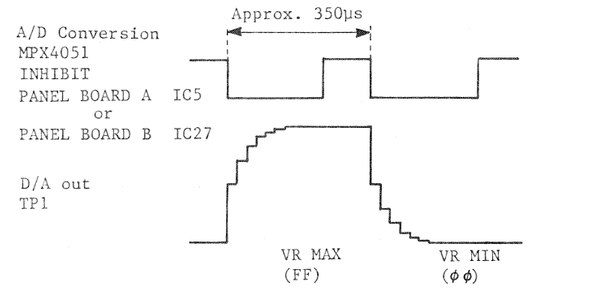
Fig. 7

ADC

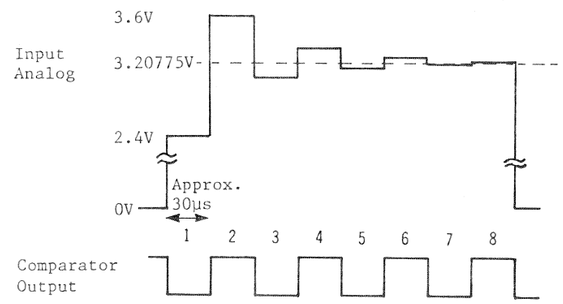
The ADC is based on a Successive Approximation consisting of DAC, comparator and CPU's internal "register". To convert a Pot value the CPU (Board B) first issues 10000000 on the data bus. IC13 latches MSB which is weighted by ladder resistors, converted to 2.4V of analog equivalent then passed on to non-inverting input pin of IC6, comparator. Being fed lower voltage on (+) input than on (–) input signal being compared, the comparator turns its output low, telling the computer to keep MSB high. Then the CPU places the next bits 11000000 which caused (+) input of the comparator to rise to 3.6V, which, in turn caused comparator output to turn high, resetting DB6 to 0.

In the same manner the CPU compares all the bits down to DB0 against the comparator's (–) input signal and establishes the digital data for that Pot value.

This procedure is repeated 16 times for all 16 pots.



The analog voltages at the VRs are converted into 8-bit digital data.



D/A Converter Input

	1	2	3	4	5	6	7	8
DB7	1	1	1	1	1	1	1	1
DB6	0	1	0	0	0	0	0	0
DB5	0	0	1	1	1	1	1	1
DB4	0	0	0	1	0	0	0	0
DB3	0	0	0	0	1	1	1	1
DB2	0	0	0	0	0	1	0	0
DB1	0	0	0	0	0	0	1	1
DBφ	0	0	0	0	0	0	0	1

Fig. 8